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10/808,615	03/25/2004	Masayuki Masuyama	67471-038	5010

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EXAMINER	
WANG, KENT F	

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2609	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/808,615	MASUYAMA ET AL.	
	Examiner	Art Unit	
	Kent Wang	2609	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8, 10-13, and 17-19* is/are rejected.

7)☐ Claim(s) *9 and 14-16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

2. The reference listed on the disclosure statement (IDS) submitted on 07/30/2004 and 02/06/2006 have being considered by the examiner (see attached PTO 1449).

Specification

3. The abstract of the disclosure is objected to because abstract should be mentioned the technique for preventing loss of shadow detail in an image underexposed due to strong incident light because that is what the improvement the invention is disclosed. Correction is required. See MPEP § 608.01(b).

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-3, 7-8, 10-13, and 19 are rejected under 35 U.S.C. § 102(e) as being anticipated by Koyama, US 2003/0151686.

Regarding claim 1, Koyama discloses an imaging device (i.e. a solid-state image pickup device) that outputs brightness information according to an amount of incident light, comprising:

- an imaging unit (i.e. a semiconductor substrate 21A) that includes a plurality of unit cells arranged one dimensionally or two-dimensionally (e.g. each pixel has an xy-address indicated by ij), each unit cell (i.e. pixel 20A) including a photoelectric conversion part (i.e. floating diode 3) that generates a first output voltage in a reset state (i.e. reset transistor 2) and a second output voltage according to an amount of incident light (i.e. amplification transistor 4), and each unit cell generating a reset voltage that corresponds to the first output voltage (i.e. reset section) and a read voltage that corresponds to the second output voltage (i.e. amplification section) (see [0057], [0058], and [0059]); and
- an output unit (i.e. voltage generation circuit 17) operable to output, in relation to each unit cell (20A), brightness information (e.g. voltage value SIG of electric charge generated by photoelectrically conversion)

indicating a difference between the reset voltage and the read voltage when the read voltage is in a predetermined range (i.e. reference potential), and brightness information indicating high brightness when the read voltage is not in the predetermined range (see [0073] and [0084]).

Regarding claim 19, Koyama discloses an imaging method for use in an imaging device that includes an imaging area formed by a plurality of unit cells (21A) arranged one dimensionally or two-dimensionally, and outputs brightness information (e.g. amplification transistor 4) according to an amount of incident light, each unit cell (20A) including a photoelectric conversion part (3) that generates a first output voltage in a reset state (i.e. reset transistor 2) and a second output voltage according to an amount of incident light (i.e. amplification resistor 4), and each unit cell generating a reset voltage corresponding to the first output voltage (e.g. reset section) and a read voltage corresponding to the second output voltage (i.e. amplification section), the method comprising:

- a judgment step of judging (e.g. when a signal output is measured for each pixel), in relation to each unit cell, whether the read voltage is in a predetermined range (e.g. if a pixel whose output is smaller than or equal to predetermined level) (see [0067]);
- a first output step (i.e. reset section) of outputting brightness information indicating a difference between the reset voltage and the

read voltage when the read voltage is judged to be in the predetermined range (e.g. between the voltage reset drain and the floating diode in terms of potential) (see [0071], [0072] and [0073]); and

- a second output step (i.e. amplification section) of outputting brightness information (e.g. a voltage VD1 of a voltage generation circuit 17) indicating high brightness when the read voltage is judged not to be in the predetermined range (e.g. the voltage VD1 ($\Delta 2$), i.e. ($\Delta + \Delta 2$)) (see [0084]).

Regarding claim 2, Koyama disclose output unit includes:

- a first output line (i.e. a column signal line 5) that is connected to the imaging unit (21A) and receives the reset voltage (i.e. reset transistor 2) and the read voltage output from each unit cell (20A) (see [0062]);
- a second output line (i.e. a horizontal signal line 12) that is connected to a circuit of a subsequent stage (i.e. output circuit 13) and outputs brightness information to the circuit of the subsequent stage ([0062]);
- a clamp capacitance (i.e. horizontal select transistor 10) that is connected in series between the first output line (5) and the second output line (12) ([0062]); and
- a bypass transistor (i.e. amplification transistor 4) that is connected in parallel with the clamp capacitance (10), and brings the first output line (5) and the second output line (12) out of conduction not to bypass the clamp capacitance (10) in a first case where a voltage applied between

terminals of the clamp capacitance is in the predetermined range, and brings the first output line (5)and the second output line (12) into conduction to bypass the clamp capacitance (10) in a second case where the voltage applied between the terminals is not in the predetermined range (see [0060], [0061], and [0062]).

Regarding claim 3, Koyama discloses the first case (e.g. situation in [0068]) is where an electric potential of the first output line is higher than a barrier potential of the bypass transistor (e.g. a voltage higher than or equal to the voltage rating of a transistor), and the second case (e.g. situation in [0067]) is where the electric potential of the first output line is equal to or smaller than the barrier potential of the bypass transistor (e.g. a pixel whose output is smaller than or equal to a predetermined level) (see [0067] and [0068]).

Regarding claim 7, Koyama discloses the bypass transistor is a depletion-mode transistor (e.g. reset transistor is a depletion-mode transistor because the drain terminal of the reset transistor 2 on each column is connected to a common drain power source line 15 as a voltage switch section) (see [0057]).

Regarding claim 8, Koyama discloses each unit cell includes:

- a light-receiving element (i.e. a floating diode 3) operable to generate charge according to an amount of incident light; a charge detecting unit

(i.e. select switch transistor 1) operable to hold the charge generated by the light-receiving element (3) and output the charge as a voltage signal; a reset transistor (2) that is connected in series between a reset terminal for supplying a reference voltage (VDD) and the charge detecting unit (1), and when a gate voltage (i.e. control terminal) is applied thereto, the reset transistor (2) is brought into conduction, so that the charge detecting unit (1) is reset to the reference voltage (VDD); and

- an amplifier transistor (i.e. an amplification transistor 4) that is connected between an amplifier terminal for supplying a reference voltage (VDD) and the first output line (5), and when a voltage signal converted by the charge detecting unit (1) is applied to a gate thereof, the voltage signal is amplified and the amplified voltage signal is output to the first output line (5), and wherein a barrier potential of the bypass transistor is higher by a predetermined amount than an electric potential of a saturation signal that is an output of the amplifier transistor (4) and that depends on an electric potential of the reset transistor (2) being out of conduction (see [0057], [0058], and [0059]).

Regarding claim 10, Koyama discloses the output unit (17) further includes a voltage supplying unit (VDD) operable to supply a bias voltage to a gate of the bypass transistor (4), and wherein a difference between the barrier

potential of the bypass transistor (4) and the electric potential of the saturation signal is set by the bias voltage (see [0084]).

Regarding claim 11, Koyama discloses the bypass transistor (4) and the reset transistor (2) are manufactured in one process (e.g. when manufacturing solid-state image pickup devices, the solid-state image pickup devices on a wafer are uniformly illuminated to bring light to the respective floating diodes) (see [0067]).

Regarding claim 12, Koyama discloses the voltage supplying unit (VDD) includes a bias setting circuit that enables an appropriate bias unique to the imaging device to be set from outside (e.g. the electric charge is potentially shut off from the application portion of the voltage reset drain and is temporarily fixed) (see [0072]).

Regarding claim 13, Koyama discloses the reset transistor (2) is manufactured by a predetermined process of burying through injection (e.g. devices on a wafer), and the bypass transistor (4) is manufactured by the predetermined process of burying through injection and an additional injection process (e.g. devices on a wafer), and wherein a difference between the barrier potential of the bypass transistor (4) and the electric potential of the saturation signal is set by the additional injection process (e.g. when manufacturing solid-state image pickup devices, the solid-state image pickup

devices on a wafer are uniformly illuminated to bring light to the respective floating diodes) (see [0067]).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 4-5 and 17-18 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Koyama in view of Rhodes, US 2001/0012225.

Regarding claim 4, Koyama disclose an output unit (output circuit 13 or 17) for an imaging device. Koyama does not does not explicitly disclose the output unit further includes a sampling capacitance, a clamping transistor, and a control unit.

Rhodes discloses the output unit (i.e. readout circuit 60) further includes:

- a sampling capacitance (i.e. a signal storage capacitor 74) that is connected in series between the second output line and a terminal for supplying a predetermined voltage ([0014]);
- a clamp transistor (i.e. a S/H transistor 72) that is connected in series between the second output line and a terminal for supplying a reference voltage ([0014]); and

- a control unit (i.e. control circuit 250) operable to control a reset voltage (i.e. reset transistor 31) to be output to the first output line (i.e. line 42) in a state where the clamp transistor (72) is ON and the second output line (i.e. VOUTS) is set at the reference voltage (i.e. supply voltage VDD), and then control a read voltage (i.e. follower transistor 36) to be output to the first output line (42) in a state where the clamp transistor (72) is OFF, (e.g. the control circuit 250 control address decoders for selecting appropriate row and column lines for pixel readout) (see [0016]) and
- wherein when a reset voltage (31) that is in the predetermined range is output to the first output line (42) in a state where the clamp transistor (72) is ON and the second output line (VOUTS) is set at the reference voltage, an equivalent to a difference between the reference voltage (VSS) and the reset voltage (31) is held by the clamp capacitance (72), and then when a read voltage (36) that is in the predetermined range (VDD) is output to the first output line in a state where the clamp transistor is OFF, a voltage of the second output line (VOUTS) changes from the reference voltage (VSS) by an amount corresponding to the equivalent held by the clamp capacitance (74), so that brightness information indicating a difference between the reset voltage (31) and the read voltage (36) is output, and
- when a read voltage (36) that is not in the predetermined range (VDD) is output to the first output line (42) in a state where the clamp

transistor (72) is OFF, the bypass transistor (i.e. S/H transistor 62) brings the first output line (42) and the second output line (VOUTS) into conduction to bypass the clamp capacitance (74) and so the voltage of the second output line is replaced by the read voltage (36), so that brightness information indicating high brightness is output regardless of whether the reset voltage (31) is in the predetermined range(VDD) (see [0013], [0014], and [0015]).

Koyama and Rhodes are analogous art because they are from the same field of endeavor of solid-state image pickup device. At the time of the invention, it would have been obvious to a person of the ordinary skill in the art to use Rhodes' output unit in Koyama's solid-state image pickup device. The suggestion/motivation would have been to enable a signal called "reset sample and hold" briefly turns on the bypass transistor immediately after the reset signal has caused reset transistor to turn on and reset the potential of the floating diffusion node, so that the capacitor stores the voltage to which the floating diffusion node has been reset ([0014]).

Regarding claim 5, Koyama disclose output unit for an imaging device. Koyama does not does not explicitly disclose the output unit further includes a sampling capacitance, a clamping transistor, and a control unit.

Rhodes discloses the output unit (60) further includes:

- a sampling capacitance (74) that is connected in series between the second output line and a terminal for supplying a predetermined voltage ([0014]);
- a clamp transistor (72) that is connected in series between the second output line and a terminal for supplying a reference voltage ([0014]); and
- a control unit (250) operable to control a reset voltage (31) to be output to the first output line (42) in a state where the clamp transistor (72) is ON and the second output line (VOUTS) is set at the reference voltage (VDD), and then control a read voltage (36) to be output to the first output line (42) in a state where the clamp transistor (72) is OFF, and
- wherein when the clamp transistor (72) is switched ON in a state where a read voltage (36) that is in the predetermined range (VDD) is output to the first output line (42), an equivalent to a difference between the reference voltage (VSS) and the read voltage (36) is held by the clamp capacitance, and then the clamp transistor (72) is switched OFF and a reset voltage (31) that is in the predetermined range (VDD) is output to the first output line (42); and a voltage of the second output line (VOUTS) changes from the reset voltage (31) by an amount corresponding to the equivalent held by the clamp capacitance (72), so that brightness information indicating a difference between the reset voltage (31) and the read voltage (36) is output, and

- the bypass transistor (62) brings the first output line (42) and the second output line (VOUTS) into-conduction to bypass the clamp capacitance (72) in a state where a read voltage (36) that is not in the predetermined range (VDD) is output to the first output line (42) and so no voltage is held by the clamp capacitance (72), so that brightness information indicating high brightness is output (see [0013], [0014], and [0015]).

Koyama and Rhodes are analogous art because they are from the same field of endeavor of solid-state image pickup device. At the time of the invention, it would have been obvious to a person of the ordinary skill in the art to use Rhodes' output unit in Koyama's solid-state image pickup device. The suggestion/motivation would have been to enable the capacitor stores the voltage to which the floating diffusion node has been reset, thereby provides correlated sampling of the potential of the floating diffusion node ([0014]).

Regarding claim 17, Koyama disclose an output unit for an imaging device. Koyama does not does not explicitly disclose the output unit further includes a sampling transistor and a sampling transistor control unit.

Rhodes discloses the output unit (60) further includes

- a sampling transistor (i.e. a S/H transistor 72) that is connected in series between the first output line (42) and the clamp capacitance (i.e. a signal storage capacitor 74); and

- a sampling transistor control unit (i.e. control circuit 250) operable to bring the sampling transistor (72) out of conduction in a vertical blanking period during which brightness information is not output from the imaging unit (see [0013] and [0016]).

Koyama and Rhodes are analogous art because they are from the same field of endeavor of solid-state image pickup device. At the time of the invention, it would have been obvious to a person of the ordinary skill in the art to use Rhodes' output unit in Koyama's solid-state image pickup device. The suggestion/motivation would have been to enable the control unit to control address encoders for selecting the appropriate row and column lines for pixel readout and thereby to improve the operating speed of the transistors used in a CMOS imager ([0001] and [0020]).

Regarding claim 18, Koyama disclose each unit cell further includes:

- an amplifier transistor (4) that is connected in series between an amplifier terminal for supplying a reference voltage (VDD) and the first output line (5), and when a voltage signal converted by a charge detecting unit (1) is applied to a gate thereof, the voltage signal is amplified and the amplified voltage signal (4) is output to the first output line (5) (see [0057]); and
- a select transistor (1) that is connected in series between the amplifier terminal and the amplifier transistor (4) or between the amplifier transistor and the first output line (5), and the

- output unit (13 or 17) (see [0057]).

Koyama does not does not explicitly disclose the output unit includes a load transistor and a control unit.

Rhodes discloses each unit cell further includes:

- a load transistor (i.e. a load transistor 39) operable to read the output voltage via the amplifier transistor (36) and the select transistor by loading the first output line (42) when the load transistor is in conduction ([0012]); and
- a control unit operable to
  (a) bring a select transistor (38) included in one or more of the unit cells into conduction before bringing the load transistor (39) into conduction,
  (b) bring the load transistor (39) out of conduction before bringing select transistors (38) included in all the unit cells out of conduction, and
  (c) bring the load transistor (39) out of conduction during a vertical blanking period during which brightness information is not output from any of the unit cells (see [0011] and [0012]).

Koyama and Rhodes are analogous art because they are from the same field of endeavor of solid-state image pickup device. At the time of the invention, it would have been obvious to a person of the ordinary skill in the art to use Rhodes' output unit in Koyama's solid-state image pickup device. The suggestion/motivation would have been to improve the speed of the

transistor gates and selectively removing the silicide or barrier from a photogate to prevent blockage of the photogate, thereby provide a silicide coating over the transistor gates used in a CMOS imager to improve the operating speed of the transistor (see [0001] and [0020]).

8. Claim 6 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Koyama in view of Park, US 7,088,393.

Regarding claim 6, Koyama disclose output unit. Koyama does not does not explicitly disclose a voltage supplying unit operable to supply a bias voltage to a gate of the bypass transistor.

Park discloses a voltage supplying unit (i.e. a secondary power supply voltage VDD) operable to supply a bias voltage to a gate of the bypass transistor (i.e. driving transistor M21) (see col. 5, lines 54-67).

Koyama and Park are analogous art because they are from the same field of endeavor of solid-state image pickup device. At the time of the invention, it would have been obvious to a person of the ordinary skill in the art to use Park's bias voltage power supply in Koyama's solid-state image pickup device. The suggestion/motivation would have been to enable the power gain of the circuit can be boosted by the action of the capacitance and the feedback circuit by boosting the effective bias voltage applied the drain terminal of the transistor (see col. 5, lines 54-67).

Allowable Subject Matter

9. Claims 9, 14, 15, and 16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- Fossum et al. (US 6,194,696) discloses a current mode device for an active pixel sensor includes a voltage to current converter which includes an operation that occurs inside a source follower.
- Ahn et al. (US 2003/0174226) discloses an image sensor with an improved automatic control of a reset voltage so that the image sensor itself automatically controls a proper clamping voltage in accordance with changes in external environments and processes and a control method thereof.
- Miyagawa et al. (US 5,504,526) discloses a solid-state imaging device includes a substrate, and an array of charge-packet storage cells or picture elements arranged on the substrate, each including a storage diode that stores therein a signal charge packet indicative of an incident light.
- Washkurak et al. (US 6,704,050) discloses a solid-state imaging device including a large array of pixels which can be fabricated

using a CMOS process and which yields a signal with lower levels of fixed-pattern noise caused by pixel-to-pixel variation in operating parameters including voltage variations on the column and output busses.

Inquiries

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kent Wang whose telephone number is 571-270-1703. The examiner can normally be reached on 8:00 A.M. - 5:30 PM (every other Friday off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chanh Nguyen can be reached on 571-272-7772. The fax phone number for the organization where this application or proceeding is assigned is 571-270-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Kent Wang

21 May 2007

CHANH D. NGUYEN
SUPERVISORY PATENT EXAMINER